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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/707,677	01/02/2004	Ko-Hsing Chang	12089-US-PA	1676	
31561	7590 08/24/2005		EXAM	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE			SOWARD	SOWARD, IDA M	
7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2		ART UNIT	PAPER NUMBER		
TAIPEI, 100			2822		
TAIWAN			DATE MAILED: 08/24/200	DATE MAILED: 08/24/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)						
Office Action Summary		10/707,677	CHANG ET AL.						
		Examiner	Art Unit						
		Ida M. Soward	2822						
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply									
THE - Exter after - If the - If NC - Failu Any (ORTENED STATUTORY PERIOD FOR REPL MAILING DATE OF THIS COMMUNICATION. nsions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. period for reply specified above is less than thirty (30) days, a repl operiod for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	I36(a). In no event, however, may a reply be ting ly within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDONE	nely filed rs will be considered timely the mailing date of this co ED (35 U.S.C. § 133).						
Status									
1)	Responsive to communication(s) filed on 14 Ju	une 2005							
′=	This action is FINAL . 2b) This action is non-final.								
,	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
5)□ 6)⊠ 7)□	Claim(s) 7-15 is/are pending in the application 4a) Of the above claim(s) is/are withdraw Claim(s) is/are allowed. Claim(s) 7-15 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/or	wn from consideration.							
Applicati	on Papers								
9)□	The specification is objected to by the Examine	er.							
10)[D)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.								
	Applicant may not request that any objection to the	drawing(s) be held in abeyance. See	e 37 CFR 1.85(a).						
_	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11)[The oath or declaration is objected to by the Ex	xaminer. Note the attached Office	Action or form PT	O-152.					
Priority u	ınder 35 U.S.C. § 119								
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 									
Attachmen		<u> </u>							
	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summary Paper No(s)/Mail Da							
3) 🔲 Inforr	e of Dransperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date		Patent Application (PTO)-152)					

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DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed June 14, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Noguchi et al. (US 2003/0042558 A1).

In regard to claim 7, Noguchi et al. teach a multi-level memory cell comprising: a substrate 1; a gate 5 disposed over the substrate 1; a source region 10 and a drain region 9 configured in the substrate 1 on each side of the gate 5; a tunneling dielectric layer 2 disposed between the gate 5 and the substrate 1; a charge-trapping layer 3 disposed between the tunneling dielectric layer 2 and the gate 5; and a top dielectric layer 4 disposed between the charge-trapping layer 3 and the gate 5, wherein the top dielectric layer 4 has at least two portions from the source region 10 to the drain region 9, and the portions have different thicknesses, and wherein the tunneling dielectric layer

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2 has substantially the same thickness from the source region 10 to the drain region 9 (Figure 1, pages 2-3, paragraphs [0041]-[0051]).

In regard to claim 8, Noguchi et al. teach a material constituting the charge-trapping layer 3 comprising silicon nitride (Figure 1, page 2, paragraph [0042]).

In regard to claim 9, Noguchi et al. teach the cell further comprising a pair of spacers 8 disposed on each sidewall of the gate 5 (Figure 1, page 3, paragraph [0048]).

In regard to claim 10, Noguchi et al. teach the cell further comprising lightly doped regions 38 & 50 configured in the substrate 1 underneath the spacers 8 (Figure 12H, pages 11-12, paragraphs [0155] and [0157], respectively).

In regard to claim 11, Noguchi et al. teach material constituting the spacers 8 comprises silicon oxide (Figure 1, page 3, paragraph [0048]).

In regard to claim 12, Noguchi et al. teach the tunneling dielectric layer 2 having a thickness of 0.5 to 10 nm (~ 5 to 100Å) (page 2, paragraph [0041]) which fits in the range of between about 20Å to 40Å.

In regard to claim 13, Noguchi et al. teach the charge-trapping layer 3 having a thickness of 3 to 50 nm (~ 30 to 500Å) (page 2, paragraph [0042]) which fits in the range of between about 40Å to 60Å.

In regard to claim 14, Noguchi et al. teach a material constituting the tunneling dielectric layer 2 comprising silicon oxide (page 2, paragraph [0041]).

In regard to claim 15, Noguchi et al. teach a material constituting the top dielectric layer 4 comprising silicon oxide (page 2, paragraph [0042]).

Response to Arguments

Applicant's arguments with respect to claims 7-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to multi-level memory cells:

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Beaman (US 2004/0067629 A1) Eitan (US 6,649,972 B2)

Gregor et al. (US 6,008,091) Kim (US 2002/0179958 A1)

Lancaster (US 6,750,102 B1) Lee et al. (6,124,153)

Ryu et al. (US 2003/0203560 A1) Shiraiwa et al. (US 6,740,605 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS August 18, 2005

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